

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original)

An integrated circuit testing apparatus, comprising:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal of said integrated circuit and a substrate coupling effect on a plurality of components within said integrated circuit;

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value;

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path within said integrated circuit; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said integrated circuit.

Claim 2 (Original)

The apparatus of claim 1 wherein said first test circuit further comprises a first ring oscillator, said first ring oscillator being routed to mimic a data path within said integrated circuit and being powered by an external power supply.

Claim 3 (Original)

The apparatus of claim 1 wherein said second test circuit further comprises a second ring oscillator, said second ring oscillator being routed within a core logic area of said integrated circuit and being powered by an external power supply.

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Claim 4 (Original)

The apparatus of claim 1 wherein said third test circuit further comprises a third ring oscillator, said third ring oscillator being randomly located within a core logic area of said integrated circuit and being powered by an external power supply.

Claim 5 (Original)

The apparatus of claim 1 wherein said fourth test circuit further comprises a fourth ring oscillator, said fourth ring oscillator being routed to mimic a data path within said integrated circuit and sharing a power supply with a core logic area of said integrated circuit.

Claims 6 – 51 (Canceled)